Recommendations for Printed Circuit Board Assembly of Infineon P(G)-VQFN Packages

Additional Information

DS6, November 2010

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1 Package Description

The P(G)-VQFN, Plastic (Green) Very Thin Profile Quad Flat Non Leaded Package, (**Figure 1** and **Figure 2**) is a near chip-scale plastic encapsulated package. It provides on the package bottom side perimeter pads and also a large die pad, which is typically also soldered to the printed circuit board to get an optimum of electrical and thermal performance and board level reliability. **"G" denotes "green" VQFN packages, which means lead-free package material set (RoHS compliant).**

Features

- Optimized electrical performance with short leads
- Enhanced thermal performance through exposed die pad structure
- Leads and exposed die pad with solder plating
- Small footprint, thin package
- Package outline according JEDEC MO-220

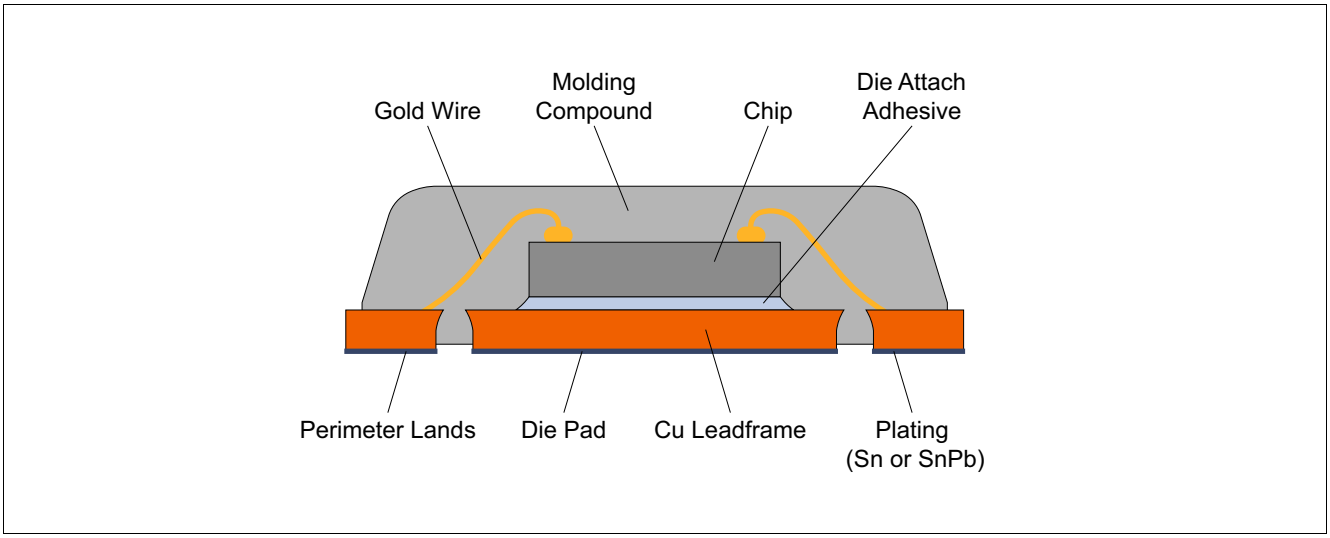


Figure 1 P(G)-VQFN Punched Type

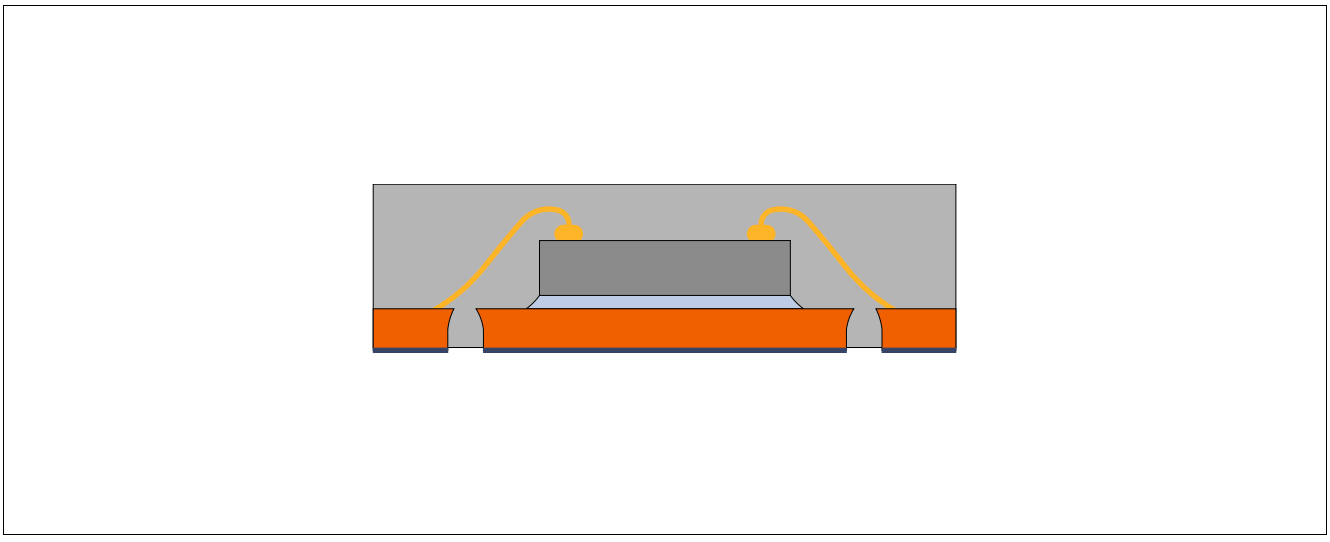


Figure 2 P(G)-VQFN Sawn Type

2 Package Handling

2.1 ESD Protective Measures

Semiconductor devices are normally electrostatic discharge sensitive devices (ESDS) requiring specific precautionary measures regarding handling and processing. Discharging of electrostatic charged objects over an IC, caused by human touch or by processing tools may cause high current respectively high voltage pulses, which may damage or even destroy sensitive semiconductor structures. On the other hand ICs may also be charged during processing. If discharging takes place too quickly (“hard” discharge), it may cause load pulses and damages, either. ESD protective measures must therefore prevent a contact with charged parts as well as a charging of the ICs. Protective measures against ESD include both the handling and processing and the packing of ESDS. A few hints are provided below on handling and processing.

2.1.1 Workplace-ESD Protective Measures

- Standard marking of ESD protected areas
- Access controls, with wrist strap and footwear testers
- Air conditioning
- Dissipative and grounded floor
- Dissipative and grounded working and storage areas
- Dissipative chairs
- Earth bonding point for wrist strap
- Trolleys with dissipative surfaces and wheels
- Suitable shipping and storage containers
- No sources of electrostatic fields

2.1.2 Equipment for Personal

- Dissipative/conductive footwear or heel straps
- Suitable smocks
- Wrist strap with safety resistor
- Volume conductive gloves or finger cots
- Regular training of staff

2.1.3 Production Installations and Processing Tools

- Machine and tool parts made of dissipative or metallic materials
- No materials having thin insulating layers for sliding tracks
- All parts reliably connected to ground potential
- No potential difference between individual machine and tool parts
- No sources of electrostatic fields

Detailed information on ESD protective measures may be obtained from the ESD Specialist through Area Sales Offices. Our recommendations are based on the internationally applicable standards IEC 61340-5-1 and ANSI/ESD S2020.

2.2 Packing of Components

List of relevant standards which should be considered

IFX packs according to the IEC 60286-* series

IEC 60286-1	Packaging of components for automatic handling - Part 1: Tape packaging of components with axial leads on continuous tapes
IEC 60286-2	Packaging of components for automatic handling - Part 2: Tape packaging of components with unidirectional leads on continuous tapes
IEC 60286-3	Packaging of components for automatic handling - Part 3: Packaging of surface mount components on continuous tapes
IEC 60286-4	Packaging of components for automatic handling - Part 4: Stick magazines for dual-in-line packages
IEC 60286-5	Packaging of components for automatic handling - Part 5: Matrix trays
IEC 60286-6	Packaging of components for automatic handling - Part 6: Bulk case packaging for surface mounting components

Moisture Sensitive Surface Mount Devices are packed according to IPC/JEDEC J-STD-033*:
Handling, Packing, Shipping and Use of Moisture/Reflow Sensitive Surface Mount Devices

Detailed packing drawings: Packing Information (Internet)

Other references

ANSI/EIA-481-*	Standards Proposal No. 5048, Proposed Revision of ANSI/EIA-481-B 8 mm through 200 mm Embossed Carrier Taping and 8 mm & 12 mm Punched Carrier Taping of Surface Mount Components for Automatic Handling (if approved, to be published as ANSI/EIA-481-C)
EIA-726	8 mm Punched & Embossed Carrier Taping of Surface Mount Components for Automatic Handling of Devices Generally Smaller than 2.0 mm x 1.2 mm
EIA-747	Adhesive Backed Punched Plastic Carrier Taping of Singulated Bare Die and Other Surface Mount Components for Automatic Handling of Devices Generally Less than 1.0 mm Thick
EIA/IS-763	Bare Die and Chip Scale Packages Taped in 8 mm & 12 mm Carrier Tape for Automatic Handling
EIA-783	Guideline Orientation Standard for Multi-Connection Package (Design Rules for Tape and Reel Orientation)

2.3 Storage and Transportation Conditions

Improper transportation and unsuitable storage of components can lead to a number of problems during subsequent processing, such as poor solderability, delamination and package cracking effects.

List of relevant standards which should be considered

IEC 60721-3-0	Classification of environmental conditions: Part 3: Classification of groups of environmental parameters and their severities; introduction
IEC 60721-3-1	Classification of environmental conditions: Part 3: Classification of groups of environmental parameters and their severities; Section 1: Storage
IEC 60721-3-2	Classification of environmental conditions: Part 3: Classification of groups of environmental parameters and their severities; Section 2: Transportation
IEC 61760-2	Surface mounting technology - Part 2: Transportation and storage conditions of surface mounting devices (SMD) - Application guide
IEC 62258-3	Semiconductor Die Products - Part 3: Recommendations for good practice in handling, packing and storage
ISO 14644-1	Clean rooms and associated controlled environments Part 1: Classification of airborne particulates

Table 1 General Storing Conditions - Overview

Product	Condition for Storing
Wafer/Die	N2 or MBB (IEC 62258-3)
Component - moisture sensitive	MBB[1)] (JEDEC J-STD-033*)
Component - not moisture sensitive	1K2 (IEC 60721-3-1)

1) MBB = Moisture Barrier Bag

Maximum storage time

The conditions to be complied with in order to ensure problem-free processing of active and passive components are described in standard IEC 61760-2.

Internet links to standards institutes

American National Standards Institute (ANSI)

Electronics Industries Alliance (EIA)

Association Connecting Electronics Industries (IPC)

3 Printed Circuit Board (PCB)

3.1 General Remarks

Generally the printed circuit board design and construction is a key factor for achieving a high board assembly yield and also sufficient reliability. Examples are PCB pad designs of for the perimeter lands and for the large central thermal pad, which is generally recommended to be soldered to the PCB for having optimum thermal, electrical, and board level reliability performance. Also the via design and board finish have to be considered.

We want to emphasize, that this document is just a guideline to support our customers in board design. Additionally, studies at the customers may be necessary for optimization, which take into account the actual PCB manufacturer's capability, the customer's SMT process, and product specific requirements.

3.2 PCB Pad Design

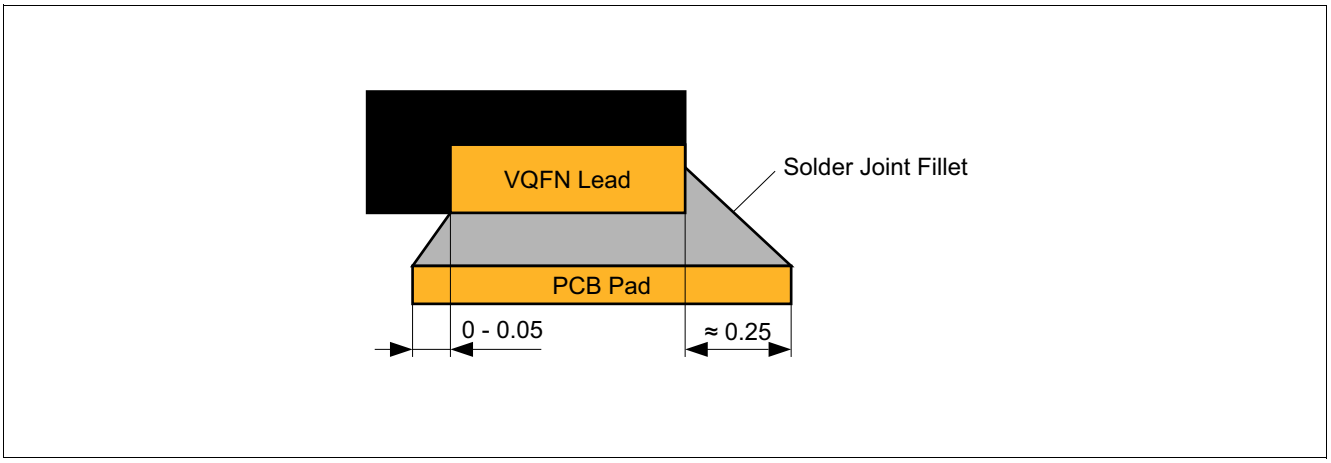


Figure 3 Schematic Cross Section of Perimeter Solder Joint

Figure 3 shows a schematic cross section of a solder joint through a perimeter land. We recommend to extend the PCB pad by ≈ 0.25 mm compared to the package land in direction of package outside. We have used this value also to calculate the pad recommendations in **Table 2 on Page 8**. This extension of the PCB pad helps to develop a solder joint fillet at the side wall of the VQFN land. However this cannot be guaranteed, as this area is not plated. Other influencing factors for fillet formation are package exposure to environment, solder paste material, and reflow process. If fillets are formed, this will additionally be beneficial for solder joint reliability. When recommending detailed PCB pad values in **Table 2** for the individual VQFN packages, we used also a slight extension of the PCB pad by 0 - 0.05 mm in direction of package center. For packages with low distance of VQFN lands and thermal die pad we have choosen the value 0, to avoid the risk of solder bridging.

As pad width we recommend 0.25 mm for pitch 0.5 mm and 0.35 mm for pitch 0.65 mm.

The VQFN packages have got a central die pad. The surface plating is the same as for the outer package pads. In most applications the die pad allows to transfer a large amount of heat into the PCB to achieve higher thermal performance. Therefore it should be soldered to the board onto the "thermal" pad. This also increases solder joint reliability and for some applications/products the electrical performance. We recommend to use die pad size on the VQFN package as maximum "thermal" pad size on the PCB (see values in **Table 2**). Slightly smaller size of the "thermal" pad is also possible.

Figure 4 shows a schematic drawing of the PCB metal design for perimeter pads and the thermal pad, which defines the important geometric parameters. In **Table 2** the details of the appropriate package specific dimensions are given.

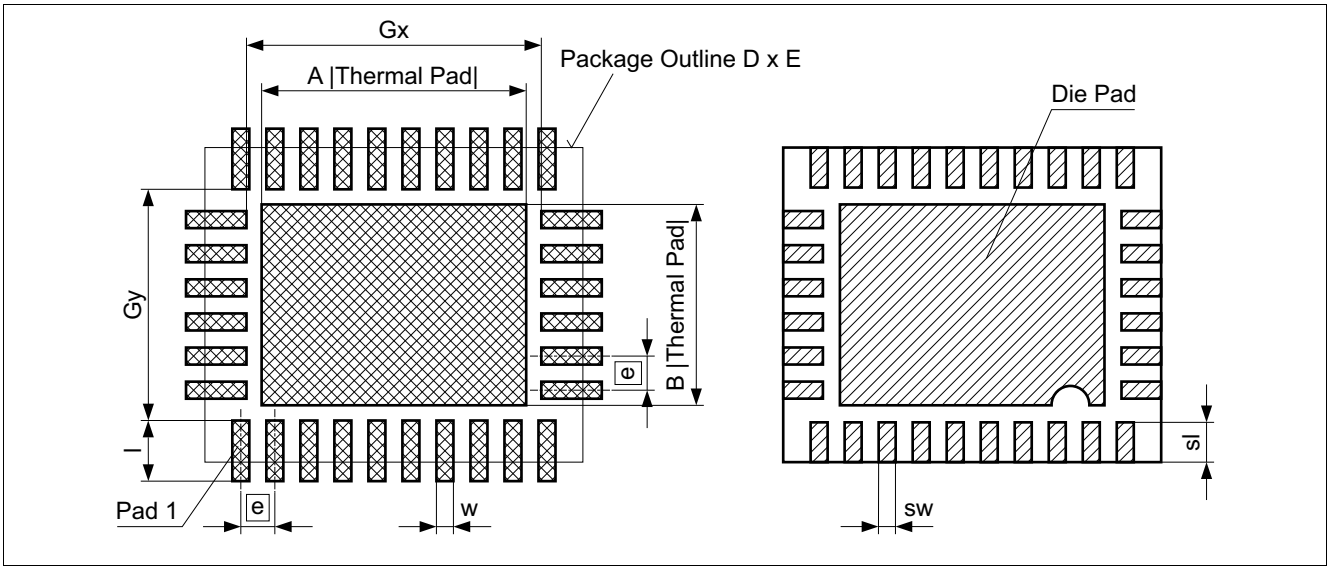


Figure 4 Schematic Drawing of PCB Pad Design Recommendation (left side) and Package Bottom View (right side)

Table 2 Recommended PCB Pad Dimensions for VQFN Packages (all dimensions in mm)

Package Name	Package Size		VQFN Perimeter Land Size on Package		Perimeter Pad Size on PCB		Max. Size of Thermal Pad on PCB		Pad Gap		Pad Pitch	Pad Number (per side)	
	D	E	sl	sw	l	w	A	B	Gx	Gy	e	nx	ny
VQFN-8-1	5.00	6.00	0.50	0.40	0.80	0.40	4.20	3.40	N.A.	4.9	1.27	4	0
VQFN-20-3	3.50	3.50	0.55	0.25	0.85	0.25	1.90	1.90	2.3	2.3	0.50	6	4
VQFN-20-6	3.50	3.50	0.60	0.20	0.85	0.25	1.90	1.90	2.3	2.3	0.50	6	4
VQFN-24-3	4.50	3.50	0.55	0.25	0.85	0.25	2.90	1.90	3.3	2.3	0.50	8	4
VQFN-24-7	4.50	3.50	0.60	0.20	0.85	0.25	2.90	1.90	3.3	2.3	0.50	8	4
VQFN-24-8	4.00	4.00	0.40	0.23	0.70	0.25	2.55	2.55	3.1	3.1	0.50	6	6
VQFN-24-13	4.00	4.00	0.40	0.23	0.70	0.25	2.50	2.50	3.1	3.1	0.50	6	6
VQFN-32-1, -5, -9	5.50	4.50	0.55	0.25	0.85	0.25	3.90	2.90	4.3	3.3	0.50	10	6
VQFN-32-3	7.00	7.00	0.55	0.35	0.85	0.35	5.00	5.00	5.8	5.8	0.65	8	8
VQFN-40-1, -8, -11	6.50	5.50	0.55	0.25	0.85	0.25	4.90	3.90	5.3	4.3	0.50	12	8
VQFN-40-2	6.50	5.50	0.55	0.25	0.85	0.25	4.90	3.90	5.3	4.3	0.50	12	8
VQFN-40-5	6.00	6.00	0.40	0.23	0.70	0.25	4.30	4.30	5.1	5.1	0.50	10	10
VQFN-48-1	7.00	7.00	0.55	0.25	0.80	0.25	5.40	5.40	5.9	5.9	0.50	12	12
VQFN-48-2, -16, -27	7.00	7.00	0.40	0.23	0.70	0.25	5.20	5.20	6.1	6.1	0.50	12	12
VQFN-48-4	7.00	7.00	0.40	0.23	0.70	0.25	5.20	5.20	6.1	6.1	0.50	12	12
VQFN-48-5	7.00	7.00	0.55	0.25	0.85	0.25	5.40	5.40	5.8	5.8	0.50	12	12
VQFN-48-6	7.00	7.00	0.40	0.23	0.70	0.25	5.20	5.20	6.1	6.1	0.50	12	12
VQFN-48-7	7.00	7.00	0.40	0.23	0.70	0.25	5.20	5.20	6.1	6.1	0.50	12	12
VQFN-48-14	9.00	9.00	0.55	0.35	0.85	0.35	6.80	6.80	7.8	7.8	0.65	12	12
VQFN-48-15, -19, -20, -22, -24, -48, -51, -52, -53, -54, -55, -56	7.00	7.00	0.40	0.23	0.70	0.25	5.20	5.20	6.1	6.1	0.50	12	12
VQFN-64-3	9.00	9.00	0.40	0.23	0.70	0.25	7.10	7.10	8.1	8.1	0.50	16	16

3.3 Solder Mask Layer

Generally, two basic types of solder pads are used.

- “Solder mask defined” (SMD) pad (**Figure 5**): The copper metal pad is larger than the solder mask opening above this pad. Thus the pad area is defined by the opening in the solder mask.

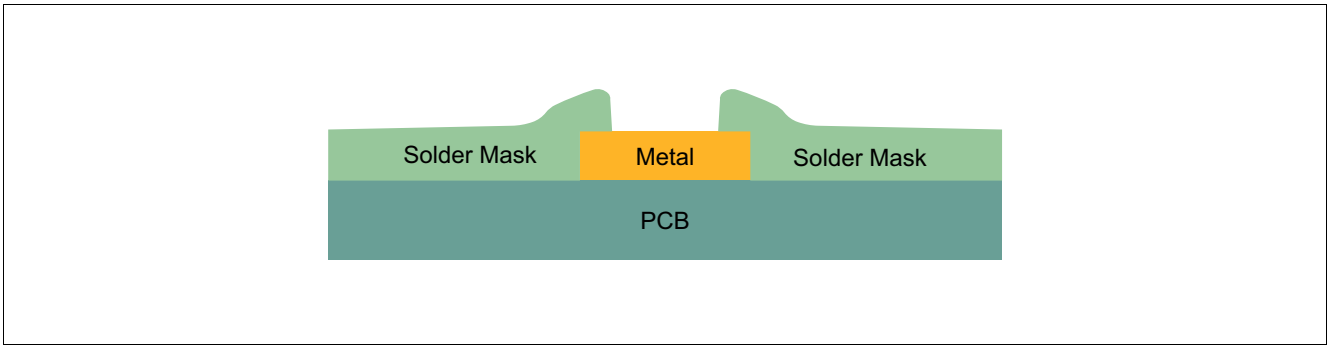


Figure 5 SMD Pad

- “Non solder mask defined” (NSMD) pad (**Figure 6**): Around each copper metal pad there is solder mask clearance. Dimensions and tolerances of the solder mask clearance have to be specified, that no overlapping of the solder pad by solder mask occurs (depending on PCB manufacturer’s tolerances, 75 µm is a widely used value).

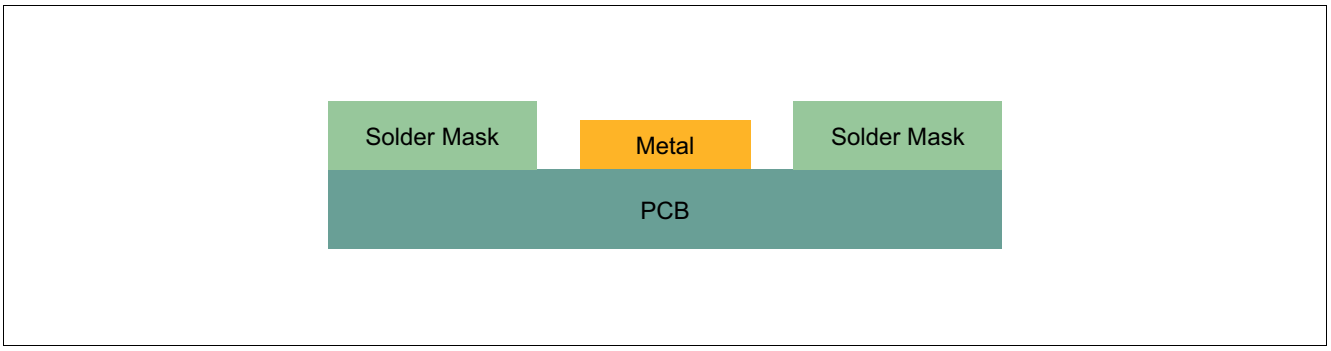


Figure 6 NSMD Pad

We recommend NSMD type for the perimeter solder pads, because the tolerances of the copper pads are lower than the solder masking process tolerances.

Between the perimeter pads on the PCB and the thermal pad in the center there should also be a ring of solder mask, which reduces the risk of solder bridging. If the distance between the perimeter pads and the metal of the thermal pad area is ≤ 300 µm, the solder mask should overlap the thermal pad metal area by ≥ 100 µm on each side.

3.4 Vias in Thermal Pad

Some products/applications require, that the “thermal” pad is connected to inner copper layers of the PCB by vias. One reason may be to maximize the electrical performance especially for products operating with high frequency. Another reason may be the optimization of the thermal performance for products having high thermal power dissipation. In this case plated through-hole vias, which are (if possible fully) connected to inner and/or bottom copper planes of the board, help to distribute the heat into the board area, which penetrates from the chip over the package die pad and the solder joint to the thermal pad on the board.

A typical via hole diameter for such thermal vias is 0.3 mm. The number of vias in the thermal pad depends on the thermal requirements of the end product, the power consumption of the product, the application, and the construction of the printed circuit board. However an array of thermal vias with pitch 1.0 - 1.2 mm can be a reasonable starting point for most products/applications for further optimization.

If the vias remain open during board manufacturing, then solder may flow into the vias during VQFN board assembly (“solder wicking”). This could have the effects of large voids in the “thermal” solder joint under the die pad, lower stand-off (which is controlled by the solder volume between package die pad and thermal pad on PCB), and/or solder protruding from the other side of the board, which may disturb a second solder paste printing process on this other board side. If necessary, the solder wicking can be avoided by plugging of the vias (filling with epoxy) or tenting the via with solder mask (e.g. with dry-film solder mask). Via tenting shall be done from top, because with via tenting from bottom side voiding rate is significantly higher.

3.5 PCB Pad Finishes

The solder pads must have good wettability to the solder paste. In general all finishes listed in **Table 4** are well proven for SMT assembly, but especially for fine pitch applications, like for VQFN packages, the quality of the plating/finish gets more important. Because of the uneven surface of Hot Air Solder Leveling (HASL) finish, lead-free or lead containing HASL is less preferred for VQFN assembly (especially for pitch < 0.65 mm) compared to completely “flat” platings like Cu-OSP (OSP: Organic Solderability Preservative) or electroless Sn or NiAu.

From package point of view it is not possible to give a definite recommendation for PCB pad finish. It also depends strongly on board design, pad geometry, all components on board, and process conditions.

4 Board Assembly

4.1 General Remarks

Many factors within the board assembly process have influence on assembly yield and board level reliability. Examples are design and material of the stencil, the solder paste material, solder paste printing process, component placement, and reflow process. We want to emphasize, that this document is just a guideline to support our customers in selection of the appropriate processes and materials. Additionally, studies at the customers may be necessary for optimization, which take into account the actual printed circuit board, the customer's SMT equipment, and product specific requirements.

Both P-VQFN with SnPb plating and lead-free PG-VQFN with Sn plating can generally be assembled with either SnPb based or lead-free SnAgCu based solder paste and reflow processes. If it is planned to assemble P-VQFN with SnPb plating with lead-free soldering process, then special attention is necessary, that the maximum specified temperature (on the moisture sensitivity caution label on the packing material) is not exceeded during processing (see also **Chapter 4.5**).

4.2 Solder Stencil

The solder paste is applied onto the PCB metal pads by screen printing. The volume of the printed solder paste is determined by the stencil aperture and the stencil thickness. In most cases the thickness of a stencil has to be matched to the needs of all components on the PCB. For VQFN packages of pitch up to 0.5 mm it is recommended to use 100 - 125 µm thick stencils. For pitch 0.65 mm also 150 µm stencil thickness is possible. If this does not match with the requirements of other packages on the same PCB, then a step-down stencil shall be considered. To ensure a uniform and high solder paste transfer to the PCB, lasercut (mostly made from stainless steel) and electroformed or electroformed stencils (Nickel) should be preferred. Rounding the corners of the apertures (radius ~50 µm) can support good paste release.

The apertures for the perimeter solder joints should be of the same size as the metal pads on the PCB (for recommendations see **Chapter 3**). The stencil in the thermal pad area shall be segmented in smaller, multiple openings (see schematic example of **Figure 7**). One large opening would result in excessive solder volume under die VQFN die pad compared to the perimeter pads as well as significantly higher voiding rate and higher risk of solder balling.

In our tests we printed a total area of about 40 - 50% of the thermal pad with solder paste. With this procedure we achieved good results in board assembly yield and reliability. The resulting solder joint stand-off was typically in the range of 50 - 60 µm. The most appropriate way of segmenting depends on the number and location of vias (if existing) and the solder resist layout on this thermal pad. In case of a regular thermal via matrix the stencil openings should be arranged in areas between the vias. In our evaluations we typically have used opening sizes ranging from 0.4 mm^2 to 1.0 mm^2, depending on via density and thermal pad size.

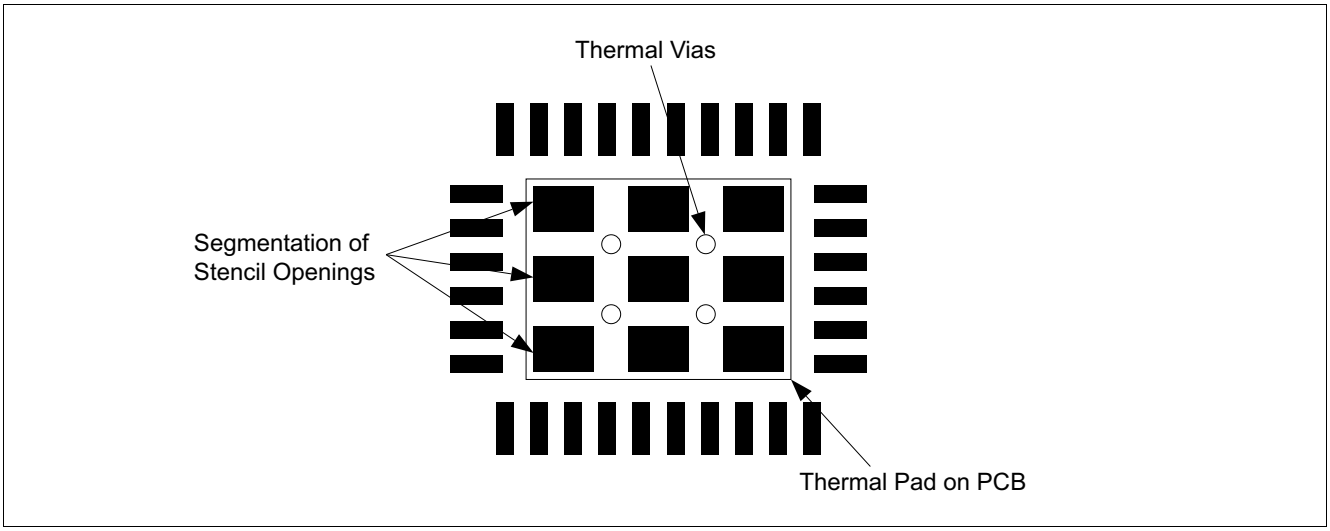


Figure 7 Example for Segmentation of Stencil Openings on Thermal Die Pad Area

4.3 Solder Paste

Solder paste consists of solder alloy and a flux system. Normally the volume is split into about 50% alloy and 50% flux. In term of mass this means approx. 90 wt% alloy and 10 wt% flux system. One of the functions of the flux system is to remove the contaminations from the solder joints during the soldering process. The capability of removing contaminations is given by the respective activation level. A lead based solder paste metal alloy has to be of leaded eutectic or near-eutectic composition (SnPb or SnPbAg). A lead-free solder paste metal alloy composition (typically SnAgCu with Ag 3 - 4%, Cu 0.5 - 1%) can also be applied. A “no-clean” solder paste is preferred, because cleaning under the soldered VQFN may be difficult. The paste must be suitable for printing the solder stencil aperture dimensions. Type 3 paste is recommended. Solder paste is sensitive to storage time, temperature and humidity. Please notice the handling recommendations of the paste manufacturer.

4.4 Component Placement

VQFN packages have to be placed accurately according to their geometry. Positioning the packages manually is not recommended.

Component placement accuracies of ±50 µm are obtained with modern automatic component placement machines using vision systems. With these systems both the PCB and the components are optically measured and the components are placed on the PCB at their programmed positions. The fiducials on the PCB are located either on the edge of the PCB for the entire PCB or additionally on individual mounting positions (local fiducials). They are detected by a vision system immediately before the mounting process. Recognition of the packages is performed by a special vision system, enabling a correct centering of the complete package.

The maximum tolerable displacement of the components is 20% of the metal pad width on the PCB (for non solder mask defined pads). In consequence, for VQFN packages the device pad to PCB pad misalignment has to be better than 50 µm to assure a robust mounting process. Generally this is achievable with a wide range of placement systems.

The following remarks are important:

- Especially on large boards local fiducials close to the device can compensate large PCB tolerances.
- It is recommended to use the lead recognition capabilities of the placement system, not the outline centering.
- To ensure the identification of the packages by the vision system, an adequate lighting as well as the correct choice of the measuring modes are necessary. The accurate settings can be taken from the equipment manuals.
- Too much placement force can lead to squeezed out solder paste and cause solder joint shorts. On the other hand too low placement force can lead to insufficient contact between package and solder paste and this can lead to open solder joints or badly centered packages.

4.5 Soldering

Soldering determines the yield and quality of assembly fabrication to a very large extent. Generally all standard reflow soldering processes

- forced convection
- vapour phase
- infrared (with restrictions)

and typical temperature profiles are suitable for board assembly of the VQFN. Wave soldering is not possible. At the reflow process each solder joint has to be exposed to temperatures above solder liquidus for a sufficient time to get the optimum solder joint quality, whereas overheating the PCB with its components has to be avoided. Please refer to the bar code label on the packing for the peak package body temperature. It is important that the maximum temperature of the VQFN package during the reflow does not exceed the specified peak temperature on the moisture level caution label on the packing of the devices (see also **Chapter 4.5.2**). When using infrared ovens without convection special care may be necessary to assure a sufficiently homogeneous temperature profile for all solder joints on the PCB, especially on large, complex boards with different thermal masses of the components, including those under the VQFN. The most recommended type is forced convection reflow. Nitrogen atmosphere can generally improve solder joint quality, but is normally not necessary for soldering tin-lead metal alloys. For the lead-free process with higher reflow temperatures, nitrogen atmosphere may reduce oxidation and improve the solder joint quality.

The temperature profile of a reflow process is one of the most important factors of the soldering process. It is divided into several phases, each with a special function. **Figure 8** shows a general forced convection reflow profile for soldering P(G)-VQFN packages, **Table 3** shows an example of the key data of such a solder profile for Tin-lead and for lead-free alloys. The single parameters are influenced by various factors, not only by the package. It is essential to follow first the solder paste manufacturer's application notes. Additionally, most PCBs contain more than one package type and therefore the reflow profile has to be matched to all components' and materials' demands. We recommend to measure the solder joints' temperatures by thermocouples beneath the respective packages. It has to be considered, that components with large thermal masses do not heat up in the same speed as lightweight components, and also the position and the surrounding of the package on the PCB, as well as the PCB thickness can influence the solder joint temperature significantly. From VQFN package point of view it has to be checked that maximum temperatures do not exceed MSL specifications, see **Chapter 4.1**.

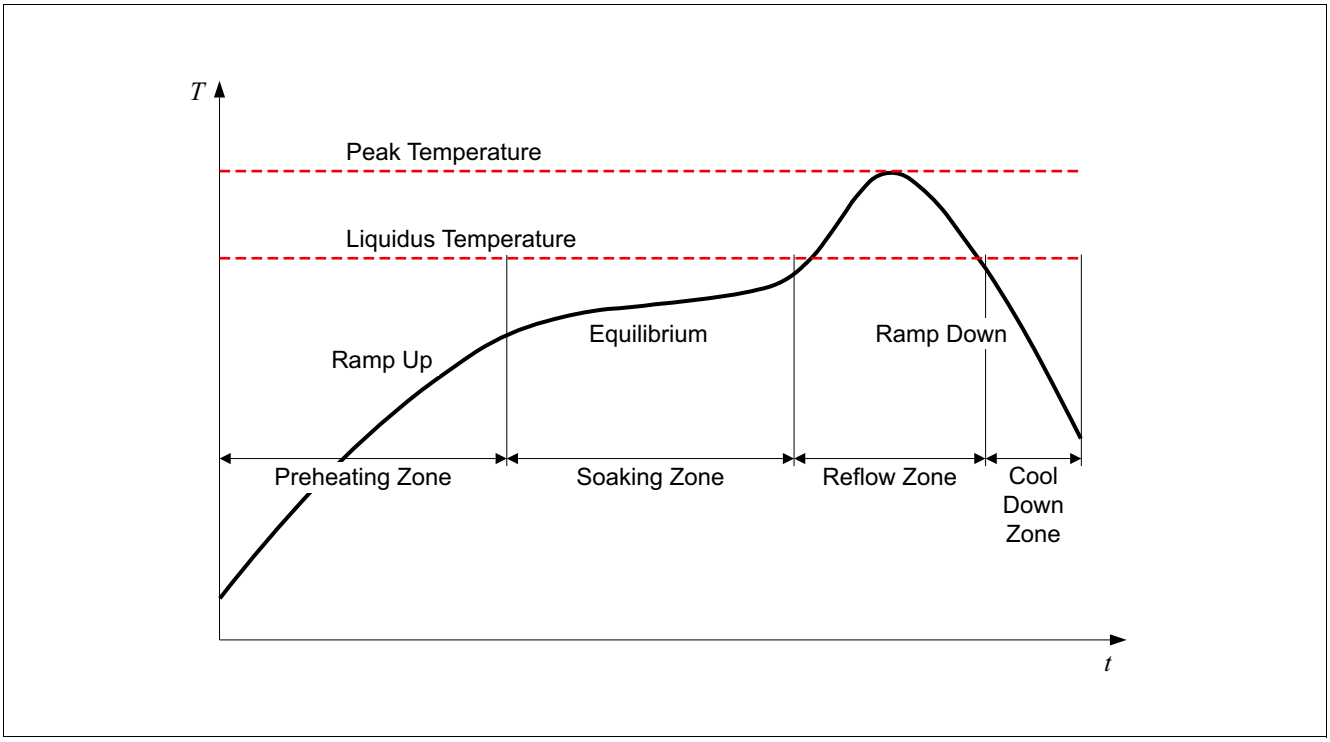


Figure 8 General Forced Convection Reflow Solder Profile

The following table is an example, not a recommendation (for reference only).

Table 3 EXAMPLE for the Key Data of a Forced Convection Reflow Solder Profile

Parameter	Tin-lead Alloy (SnPb or SnPbAg)	Lead-free Alloy (SnAgCu)	Main Requirements From
Preheating rate	2.5 K/s	2.5 K/s	Flux system (Solder paste)
Soaking temperature	140 - 170°C	140 - 170°C	Flux system (Solder paste)
Soaking time	80 s	80 s	Flux system (Solder paste)
Peak temperature	225°C	245°C	Alloy (Solder paste)
Reflow time over Liquidus	60 s	60 s	Alloy (Solder paste)
Cool down rate	2.5 K/s	2.5 K/s	

4.5.1 Double-Sided Assembly

VQFN packages are generally suitable for mounting on double-sided PCBs. That means that in a first step board assembly is done on one side of the PCB (including soldering). Afterwards the second side of the PCB is assembled.

4.5.2 Processing of Moisture-Sensitive Components

For moisture-sensitive packages like VQFN it is necessary to control the moisture content of the components. The penetration of moisture into the package molding compound is generally caused by exposure to the ambient air. In many cases moisture absorption leads to moisture concentrations in the component which are high enough to damage the package during the reflow process. Thus it is necessary to dry moisture-sensitive components, to seal them in a moisture-resistant bag and only to remove them immediately prior to board assembly to the PCB. The permissible time (from opening the moisture barrier bag until the final soldering process), which a component can remain outside the moisture barrier bag, is a measure of the sensitivity of the component to ambient humidity (Moisture Sensitivity Level, MSL). The most commonly applied standard IPC/JEDEC J-STD-033* defines eight different MSLs (see **Table 4**). Please refer to the “Moisture Sensitivity Caution Label” on the packing material, which contains informations about the moisture sensitivity level of our product. It specifies also the maximum reflow temperature, which shall not be exceeded during the board assembly at the customer.

Table 4 Moisture Sensitivity Levels (acc. to IPC/JEDEC J-STD-033*)

Level	Floor Life (out of bag)	
	Time	Conditions
1	Unlimited	≤ 30°C / 85% RH
2	1 year	≤ 30°C / 60% RH
2a	4 weeks	≤ 30°C / 60% RH
3	168 hours	≤ 30°C / 60% RH
4	72 hours	≤ 30°C / 60% RH
5	48 hours	≤ 30°C / 60% RH
5a	24 hours	≤ 30°C / 60% RH
6	Mandatory bake before use. After bake, must be reflowed within the time limit specified on the label.	≤ 30°C / 60% RH

Internet Link to **Association Connecting Electronics Industries (IPC)**

If moisture-sensitive components have been exposed to ambient air for longer than the specified time according to their MSL, or the humidity indicator card after opening the dry package indicates too much moisture, the packages have to be baked prior to the assembly process. Please refer to IPC/JEDEC J-STD-033* for details. Baking a package too often can cause solderability problems due to oxidation and/or intermetallic growth. Notice

that packing material possibly can not withstand the baking temperature. See imprints/labels on the respective packing for maximum temperature.

4.6 Cleaning

After the reflow soldering process some flux residues can be found around the solder joints. If a “no-clean” solder paste has been used for solder paste printing, the flux residues usually do not have to be removed after the soldering process. Be aware, that cleaning beneath a VQFN package is difficult because of the small gap between package and PCB and is therefore not recommended. However if the solder joints have to be cleaned, the cleaning method (e.g. ultrasonic, spray or vapor cleaning) and solution have to be selected with consideration of the packages to be cleaned, the used flux in the solder paste (rosin-based, water-soluble, etc.), environmental and safety aspects. Removing/drying even of small residues of the cleaning solution should also be done very thorough. Contact the solder paste manufacturer for recommended cleaning solutions.

4.7 Inspection

A visual inspection of the solder joints with conventional AOI (automatic optical inspection) systems is limited to the outer surface of the solder joints. Since the non-wetting of the package lead side walls is not a reject criterion, the significance of an optical inspection is poor.

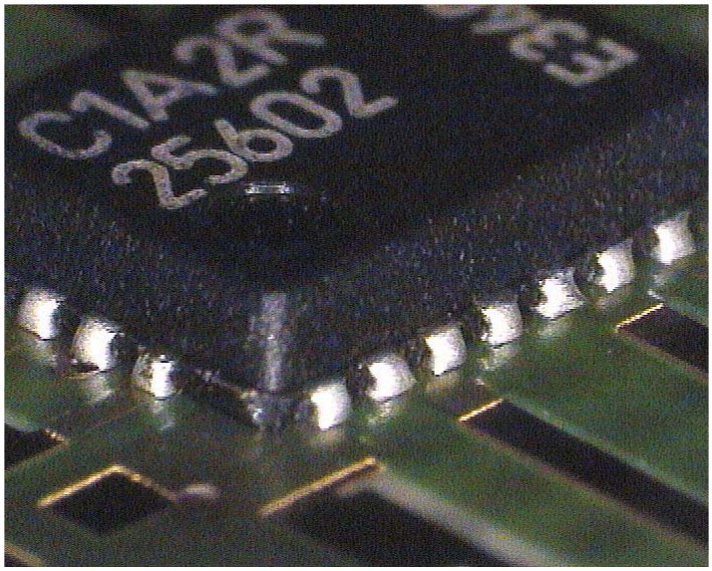


Figure 9 Overview on a Soldered VQFN Package

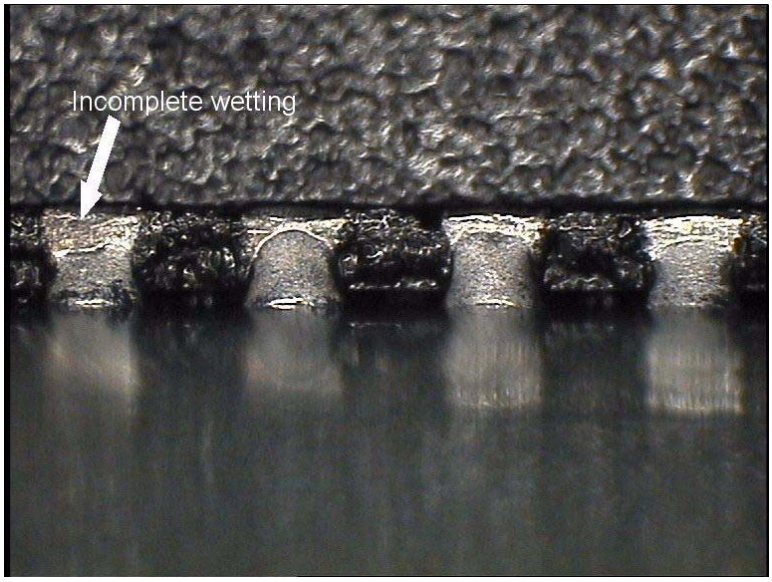
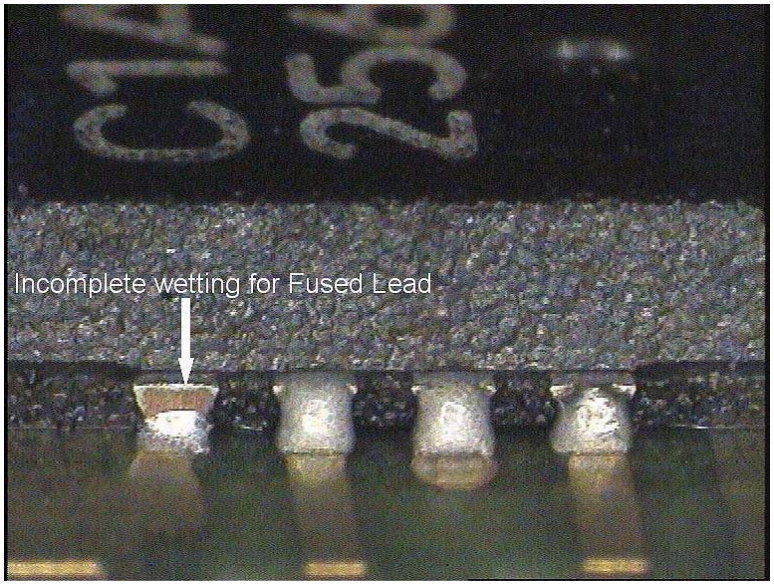


Figure 10 Non-wetting of the Lead Side Walls is not a Reject Criteria



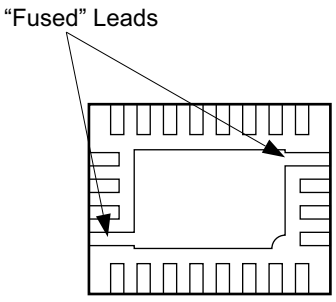


Figure 11 “Fused” leads can also show incomplete wetting of the lead side walls. This is also not a reject criterion. Fused leads denote VQFN lands, which are directly connected to the die pad via the leadframe.

The only reasonable method to realize an efficient inline control is the implementation of AXI (automatic X-ray inspection) systems. AXI systems are available as 2D and 3D solutions. They usually consist of an X-ray camera and the hard- and software needed for inspection, controlling, analysing and data transfer routines. These systems enable the user to detect soldering defects like poor soldering, bridging, voiding and missing parts quite reliable. For the acceptability of electronic assemblies please refer also to the IPC-A-610C standard.

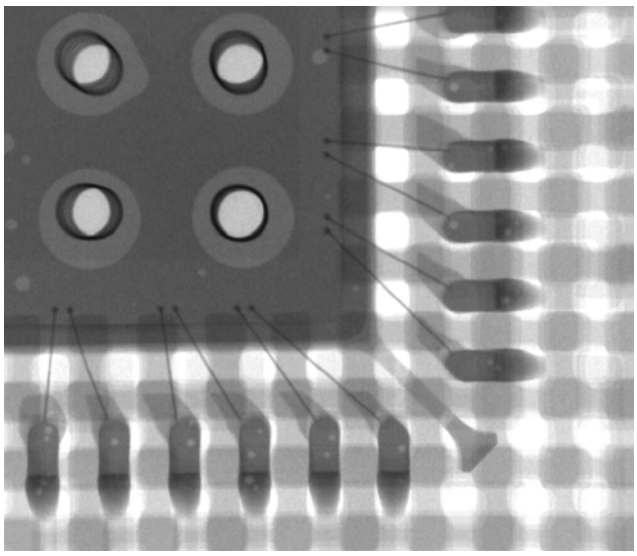


Figure 12 Typical X-ray Image of Soldered VQFN Package
Investigations have shown that voids in size and amount like in this image do not have any negative impact on reliability.

Cross sectioning of a soldered package as well as dye penetrant analysis can serve as tools for sample monitoring only, because of their destructive character.

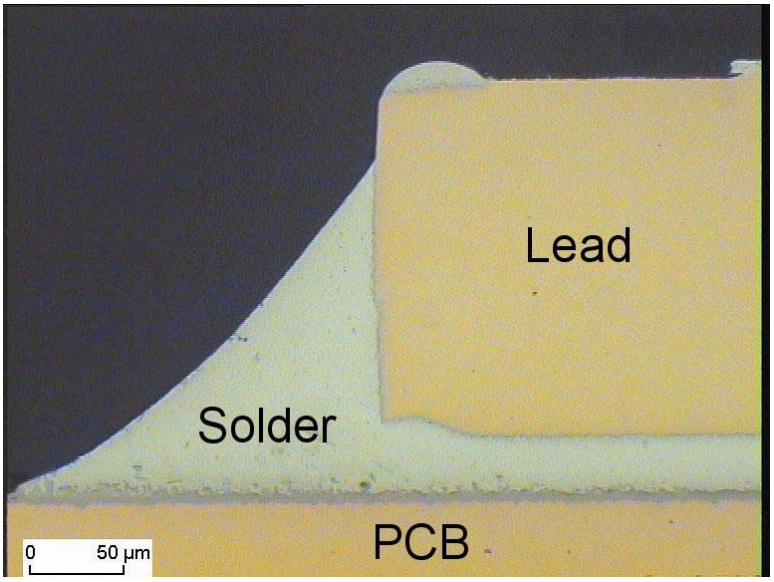


Figure 13 Cross Section of a VQFN Solder Joint

Special notes for lead-free solder joints:

Lead-free solder joints look different than tin-lead (SnPb) solder joints. Tin-lead joints have typically a bright and shiny surface. Lead-free (SnAgCu) solder joints typically do not have this bright surface. Lead-free solder joints are often dull and grainy. This surface properties are caused by the irregular solidification of the solder, as the used solder alloys are not exactly eutectic (like the 63Sn37Pb solder alloy). This means, that SnAgCu-solders do not have a melting point but a melting range of several degrees. Although lead-free solder joints have this dull surface, this does not mean that lead-free joints are of lower quality or weaker than the SnPb joints. It is therefore necessary to instruct the inspection staff, how these new lead-free joints look like, and/or to adjust optical inspection systems to lead-free solder joints.

5 Rework

If a defect component is observed after board assembly the device can be removed and replaced by a new one. Repair of single solder joints is not possible.

5.1 Tooling

The rework process is commonly done on special rework equipment. There are a lot of systems available on the market, and for processing these packages the equipment should fulfill the following requirements:

- *Heating*: Hot air heat transfer to the package and PCB is strongly recommended. Temperature and air flow for heating the device should be controlled. With free-programmable temperature profiles (e.g. by PC controller) it is possible to adapt the profiles to different package sizes and thermal masses. PCB preheating from underside is recommended. Infrared heating can be applied, especially for preheating the PCB from underside, but it should be only supporting the hot air flow from the upside. Instead of air also nitrogen can be used.
- *Vision system*: The bottom side of the package as well as the site on the PCB should be observable. For precise alignment of package to PCB a split optic should be implemented. Microscope magnification and resolution should be appropriate for the pitch of the device.
- *Moving and additional tools*: The device should be relocatable on the whole PCB area. Placement accuracy is recommended to be better than ±100 µm. The system should have the capability of removing solder residues from PCB pads (special vacuum tools).

5.2 Device Removal

If it is intended to send a defect component back to the supplier, please note that during the removal of this component no further defects must be introduced to the device, because this may hinder the failure analysis at the supplier. This includes the following recommendations:

- *Moisture*: According to his moisture sensitivity level, possibly the package has to be dried before removal. If the maximum storage time out of the dry pack (see label on packing material) is exceeded after board assembly, the PCB has to be dried according to the recommendations (see **Chapter 4.4**), otherwise too much moisture may have been accumulated and damage may occur (popcorn effect).
- *Temperature profile*: During soldering process it should be assured that the package peak temperature is not higher and temperature ramps are not steeper than for the standard assembly reflow process (see **Chapter 4.4**).
- *Mechanics*: Be aware not to apply high mechanical forces for removal. Otherwise failure analysis of the package can be impossible or PCB can be damaged. For large packages pipettes can be used (implemented on most rework systems), for small packages tweezers may be more practical.

5.3 Site Redressing

After removing the defect component the pads on the PCB have to be cleaned from solder residues. Don’t use steel brushes because steel residues can lead to bad solder joints. Before placing a new component it is recommended to apply solder paste on each PCB pad by printing (special micro stencil) or dispensing. It is recommended to use only no-clean solder paste.

5.4 Reassembly and Reflow

After preparing the site, the new package can be placed onto the PCB. The package is positioned exactly above the PCB pads, in height just that there is no contact between the package and the PCB and the package is then dropped into the printed or dispensed flux or solder paste depot (Zero-force-placement). During soldering process it should be assured that the package peak temperature is not higher and temperature ramps are not steeper than for the standard assembly reflow process (see **Chapter 4.4**).

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